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10/644,132

PATENT  
Conf. No.: 5337

IN THE UNITED STATES PATENT OFFICE

Applicants: Jason H. Anderson et al.  
Assignee: Xilinx, Inc.  
Title: Post-Layout Optimization in Integrated Circuit Design  
Serial No.: 10/644,132 File Date: 08/20/2003  
Examiner: Binh C. Tat, Art Unit: 2825  
Docket No.: X-946 US Conf. No.: 5337

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Mail Stop AMENDMENT  
COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

RESPONSE TO FIRST OFFICE ACTION

Dear Sir:

In response to the First Office Action mailed from the Patent Office on September 21, 2005, Applicants make the following remarks.

**Listing of the Claims** no amendments were made to the claims but the current claims are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks** begin on page 4 of this paper.